Chapter 3
SPACE CHARGE

3.1 Charge Neutrality

We have seen that drift current flows when a homogenous semiconductor is subjected to a uniform external electric field. In a homogenous semiconductor, n_0 and p_0 are constant independent of distance. The uniform electric field simply pushes the charge carriers such that their densities do not change with distance, but individual carriers flow around the circuit. In this case, bands tilt uniformly, and the slope of the tilt gives the electric field as in eqn. (2-39). Under these conditions charge neutrality (eqns. 2-2, 2-4) is maintained, and the field lines of the external battery stream around without change. We know that the electric field lines must originate from positive charges and terminate on negative charges. Such charges must exist on the surfaces of the metal in contact with the semiconductor, and no net charge exists in the bulk. That is why the electric field lines do not change with distance (Fig. 3.1), and hence the electric field is uniform (constant).

3.2 Equilibrium

The strict definition of equilibrium in a semiconductor is that temperature is constant, and no external stimulus or source is applied, and no net current flows for electrons or holes under all conditions (open circuit, short circuit, or with load connected), and the device is time-invariant.

Therefore, the case of a uniform electric field mentioned in the previous section cannot be considered an equilibrium condition, but it is a case of homogenous doping and uniform current carrier density under constant and uniform external electric field. We shall see (Chapter 4) that this thermal equilibrium may be disturbed also by an external stimulus. We call that condition nonequilibrium. Almost all semiconductor applications depend on device performance under such condition.

3.3 Diffusion Current

We have seen that drift current is caused by an electric field, and hence is proportional to it (eqn. 2-37), according to what is known as casue-effect sequence. Another current mechanism may exist in situations where there is a nonuniform carrier density. It is called diffusion current. It is caused by the rate of change of the difference in concentration with distance (called concentration gradient). It expresses the flow of carriers from regions of high concentration to regions of low concentration. It is purely a mechanical process and has no relation to charge or electric field. The process of diffusion can be noticed in our daily life as perfume molecules spread around in a room, until they fill the entire space, and the concentration becomes uniform all over. It stops when the concentration gradient is zero. If there are several types of molecules or different species, diffusion must be analyzed for every type independently of the others.

The process of diffusion follows from statistical considerations since in regions of high concentration collisions of particles are so frequent that they continually push these particles away from each other, thus increasing their mean free path, until a thermal equilibrium condition prevails when the particles are sufficiently and uniformly pushed apart.

We note that diffusion is an irreversible process, i.e., particles once diffused cannot gather up on their own to form back regions of high concentration, unless an external source exists, which we call injection or generation, which becomes then a case of nonequilibrium phenomenon (Chapter 4).

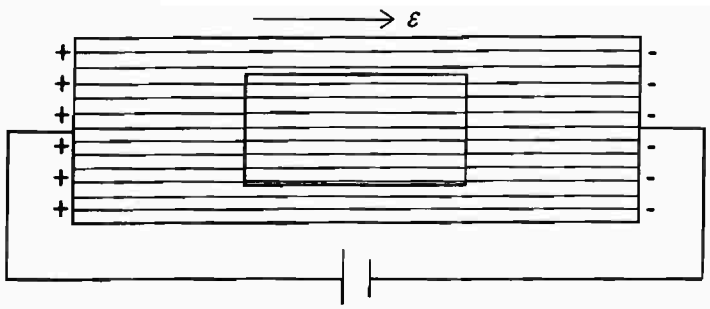

Fig. (3.1) To maintain charge neutrality electric field lines density does not change with distance

Let us now consider a semiconductor where there is a concentration gradient for holes and electrons. Hole diffusion takes place from the region of high concentration to the region of low concentration, i.e., along the positive x axis. This will give rise to a diffusion current density $J_{p_{diff}}$ proportional to the concentration gradient dp/dx

$$J_{p_{diff}} = -|q| D_p \frac{dp}{dx} \qquad (3\text{-}1)$$

Where D_p is the diffusion constant for holes. The minus sign is added since the slope dp/dx is negative as $p(x)$ decreases with x. To make the direction of current flow from the region of high concentration to the region of low concentration, i.e., along the positive x direction, the minus sign is added to correct for the sign of $\frac{dp}{dx}$

For electrons

$$J_{p_{diff}} = |q| D_n \frac{dp}{dx} \qquad (3\text{-}2)$$

where D is the diffusion constant for electrons since in this case $n(x)$ decreases with x, i.e., $\frac{dn}{dx}$ is negative. The direction is from the region of high concentration to the region of low concentration, i.e., along the positive x direction. But the current due to electrons moving along the positive x direction is along the negative x direction.

Now in general both drift and diffusion currents may exist simultaneously.

$$J_p = |q| \mu_p p \varepsilon - q D_p \frac{dp}{dx} \qquad (3\text{-}3)$$

$$J_n = |q| \mu_n n \varepsilon + q D_n \frac{dn}{dx} \qquad (3\text{-}4)$$

In the case of uniform current carrier densities, n_0 and p_0 are constant and only drift currents exist under external electric field. In the case of nonuniform current carrier densities both diffusion and drift currents exist simultaneously.

3.4 Fermi Level Under Non Uniform Concentrations

Under thermal equilibrium in the case of nonuniform densities $p_0(x)$ and $n_0(x)$, the net hole current must be zero

$$J_p = |q|\mu_p p_0(x)\varepsilon(x) - |q| D_p \frac{dp_0(x)}{dx} = 0 \tag{3-5}$$

$$\varepsilon(x) = \frac{D_p}{\mu_p}\frac{1}{p_0(x)}\frac{dp_0(x)}{dx} \tag{3-6}$$

From eqn. (2-39), defining $U(x)$ as PE

$$\varepsilon(x) = \frac{1}{q}\frac{dU(x)}{dx} = \frac{1}{q}\frac{dE_{F_i}(x)}{dx} \tag{3-7}$$

From eqn. (2-28)

$$p_0(x) = n_i e^{\left[E_{F_i}(x) - E_F(x)\right]/kT} \tag{3-8}$$

$$\frac{dp_0(x)}{dx} = n_i e^{\left[E_{F_i}(x) - E_F(x)\right]/kT}\left[\frac{dE_{F_i}(x)}{dx} - \frac{dE_F(x)}{dx}\right]$$

$$\varepsilon(x) = \frac{D_p}{\mu_p}\frac{1}{kT}\left[\frac{dE_{F_i}(x)}{dx} - \frac{dE_F(x)}{dx}\right] \tag{3-9}$$

Equating this with eqn. (3-7)

$$\frac{D_p}{\mu_p}\cdot\frac{1}{kT}\left[\frac{dE_{F_i}(x)}{dx} - \frac{dE_F(x)}{dx}\right] = \frac{1}{|q|}\frac{dE_{F_i}(x)}{dx} \tag{3-10}$$

From this equation we conclude that

$$\frac{dE_F(x)}{dx} = 0 \tag{3-11}$$

which means that $E_F(x)$ is constant throughout. We also conclude that

$$\frac{D_p}{\mu_p} = \frac{kT}{|q|} = V_{th} = \frac{D_n}{\mu_n} \tag{3-12}$$

where V_{th} is called thermal potential. Eqn. (3-12) is called Einstein's relation. It shows that semiconductor constants, namely diffusion constant and mobility are intimately related, and their ratio is governed by temperature. Note that both D_p and μ_p are statistical properties and it is logical that they are related for a given material.

3.5 Diffusion Potential

With E_F constant, and using eqn. (3-10), eqn. (3-5) reduces to

$$\varepsilon(x) = V_{th}\frac{1}{p_0(x)}\frac{dp_0(x)}{dx} \tag{3-13}$$

Since

$$\varepsilon(x) = -\frac{dV(x)}{dx} \tag{3-14}$$

We have

$$-\frac{dV}{dx} = V_{th}\frac{1}{p_0(x)}\frac{dp_0(x)}{dx} \tag{3-15}$$

$$-\frac{dV(x)}{V_{th}} = \frac{1}{p_0(x)}dp_0(x) \tag{3-16}$$

Integrating from point (1) to point (2)

$$\int_1^2 \frac{dV(x)}{V_{th}} = -\int_1^2 \frac{dp_0(x)}{p_0(x)} \tag{3-17}$$

$$\frac{V(2)-V(1)}{V_{th}} = \frac{\Delta V}{V_{th}} = -\ell n\left(\frac{p_0(2)}{p_0(1)}\right) = \ell n\left(\frac{p_0(1)}{p_0(2)}\right) \tag{3-18}$$

$$\frac{p_0(2)}{p_0(1)} = e^{-\Delta V/V_{th}} = e^{-(V_2-V_1)/V_{th}} \tag{3-19}$$

Similarly we can find (Prob. 3-1)

$$\frac{n_0(2)}{n_0(1)} = e^{\Delta V/V_{th}} = e^{(V_2-V_1)/V_{th}} \tag{3-20}$$

Clearly we find

$$p_0(2)n_0(2) = p_0(1)n_0(1) = n_i^2 \tag{3-21}$$

which is the mass action law

3.6 Diffusion Potential Dilemma

In non uniform carrier densities we have concentration gradient, which gives rise to diffusion current. Because $J_{p_{net}} = 0$ and $J_{n_{net}} = 0$, hole drift current and electron drift current must exist opposite to the diffusion currents to make the net current zero for each type of carriers. The existence of drift current requires the existence of an electric field, which requires in turn the existence of potential difference ΔV. But there is no battery since the case considered is that of thermal equilibrium. Therefore, this voltage is called built-in voltage (or diffusion voltage or contact potential or barrier potential or surface potential). Now we try to measure this voltage by connecting a voltmeter across the semiconductor. To our surprise the voltmeter reads zero. In fact we should not be surprised at that result. We should be surprised otherwise. First of all there is no net current flow whether we connect a wire (short circuit) or a voltmeter (high resistance). The voltmeter reading is based on a small current flow. Thus, it must read zero since the net current is zero. This is in agreement with our previous conclusion that Fermi level is constant. We know by now that Fermi level differences measure external voltages or create voltages that can be externally measured.

Our conclusion that the potential barrier cannot be measured by a voltmeter is in harmony with the law of conservation of energy. For if there were indeed a voltmeter reading then current would be flowing, and if we put a load (resistance) we could obtain power. Then we must wonder-in fact be alarmed where this power came from. Of course there are other indirect ways of measuring this contact potential, but for now we are speaking of the direct way of connecting a dc voltmeter across the semiconductor. Accordingly, we must - hard as it is - to accept the fact that an internal voltage and also an internal electric field exist as a result of the diffusion process and that this voltage and electric field are needed to create a state of balance in which the net current is zero and yet cannot be directly measured.

3.7 Band Bending and Space Charge

Consider a p-type semiconductor with region (1) of high concentration of holes and region (2) of low concentration of holes. As a result of eqn. (3-18), ΔV is positive, i.e., $V_1 < V_2$. Since we plot the energy band diagram for electrons, $PE_1 > PE_2$. The band edges bend upward as we go out from the inside (bulk) toward the surface, while E_i remains constant throughout (Fig. 3.2).

We note that as the bands bend upward toward the surface, the valence band edge E_v gets closer to Fermi level (which is constant) at the surface than at the bulk. Since Fermi level indicates which type of charge carrier has higher density as it gets closer to the corresponding band edge, we conclude that at the surface $p_0(1) > p_0(2)$ or $n_0(1) < n_0(2)$. The electric field varies with distance, noting that it is the slope of the energy band edges. It is higher at the surface and weaker in the bulk. Since it is directed from the bulk toward the surface, it means that as we go from the bulk toward the surface we meet more holes which produce electric field lines (since holes are positive charges) thus, increasing the magnitude of the electric field. We assume in this discussive that the doping profile, i.e. acceptor ion distribution is uniform and has nothing to do with non uniformity of holes. The band edges in this case bend upwards at the surface.

This automatically means that charge neutrality no longer holds. Thus we have a net charge. This charge is called space charge. We have not yet explained why this non uniform charge distribution exists in the first place but we will do that shortly. This band bending is contrasted with the case of band tilting in which a uniform external electric field exists and no diffusion current flows with the condition of charge neutrality holding. That is why we distinguish between band bending and band tilting (Fig. 3.3)

The bending of the bands denotes directly the existence of internal voltage difference (or barrier) and the existence of electric field, and hence the invalidation of charge neutrality, and consequently the existence of space charge. But again the constancy of Fermi level denotes the inability to measure this voltage by a voltmeter. This barrier is called surface potential.

3.8 MOS Capacitor

It is a structure composed of a metal and a semiconductor separated by an oxide, hence called metal oxide-semiconductor (MOS). As such it resembles a capacitor, except that the second capacitor terminal is a semiconductor instead of a metal (Fig. 3.4). Due to thermal equilibrium and in absence of any external voltage, Fermi levels in both metal and the semiconductor (assumed to be p-type in this case) are aligned. We shall neglect for the moment work function difference in both metal and semiconductor. But we define for convenience a modified work function for the metal oxide interface $|q|\psi_m$ which is measured from the metal Fermi level to the conduction band of the oxide. Similarly, $|q|\psi_s$ is the modified work function at the semiconductor oxide interface. In the case we assume $\psi_m = \psi_s$. Also, $|q|\psi_F$ measures the position of Fermi level below the intrinsic level E_{F_i} for the semiconductor (Fig. 3.4b). We now apply a negative votage between the metal and the semiconductor (Fig. 3a). This requires a negative charge to be deposited on the metal. An equal and opposite (positive) charge must be accumulated at the surface of the semiconductor. Since the semiconductor is p-type the positive charge comes about from the accumulation of holes. Charge neutrality requires that the negative charge (electrons) go through the wire and the battery to the metal side. Since the negative voltage at the metal side means higher potential energy at the metal side, Fermi level in the metal E_{F_M} becomes higher than Fermi level in the semiconductor by an amount $|q|V_G$ where V_G is the applied voltage.

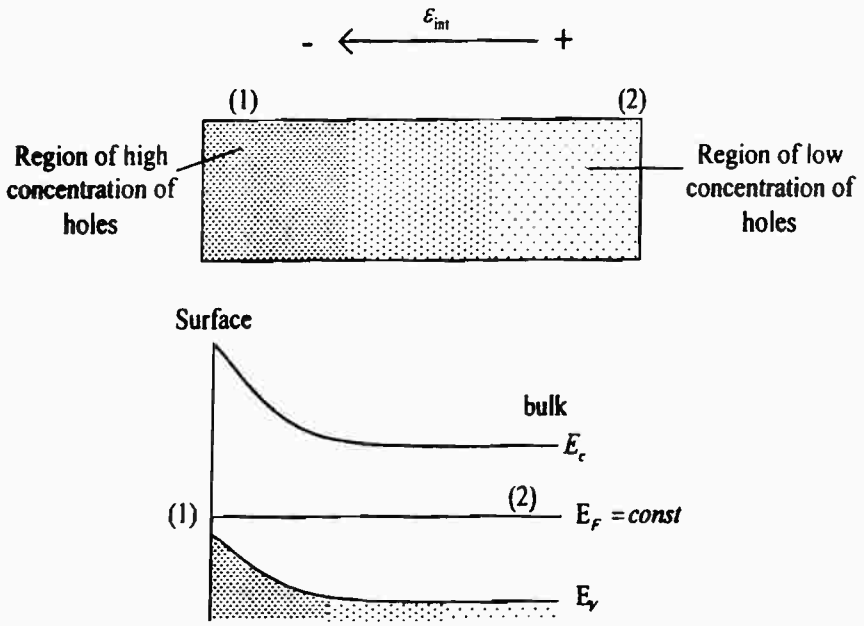

Fig. (3.2) Band bending in non uniform carrier distribution and thermal equilibrium

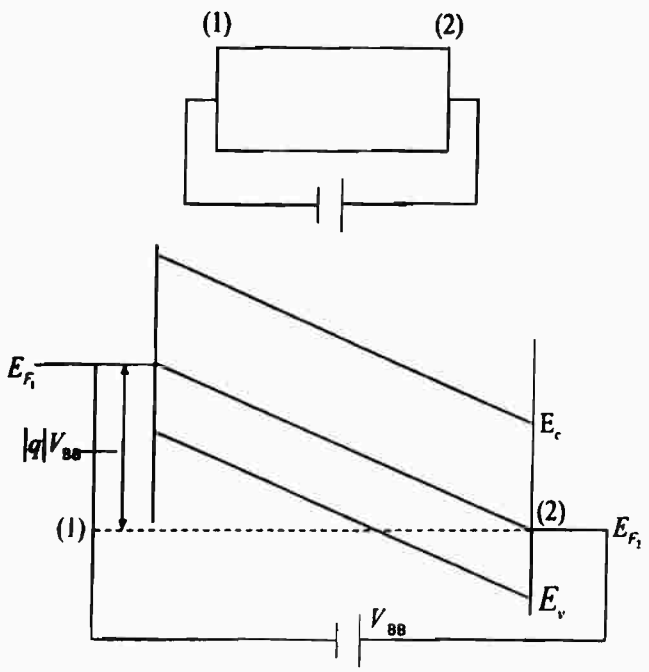

Fig. (3.3) Band tilting in uniform carrier distribution and uniform external electric field

This causes a tilt in the oxide conduction band. This is expected since an electric field due to the difference in Fermi level $E_{F_M} - E_{F_s}$ exists in the oxide. Also, band bending must take place in the semiconductor to accumulate enough space charge needed for the capacitor action. We note that E_V becomes closer to Fermi level in the semiconductor at the surface which is still E_{F_s} and hence the semiconductor becomes more p-type at the surface. This is consistent with eqn. (2-28) due to the increase in $\left(E_{F_i} - E_{F_s}\right)/kT$. The hole concentration is given by

$$p = n_i e^{\left(E_{F_i} - E_{F_s}\right)/kT} \tag{3-22}$$

where E_{F_i} and p are function of distance measured outwardly

We note that Fermi level is constant in the semiconductor since no current flows across the structure due to the presence of the oxide (insulator). Hence, as $(E_{F_i} - E_{F_s})/kT$ increases E_{F_i} moves up in energy at the surface, or E_V moves up closer to E_{F_s} which means more holes are accumulated at the surface. This is why this mode is called accumulation mode.

Now we apply a positive voltage (positive gate voltage V_G) on the metal instead of the negative gate voltage. The increase in the potential of the metal means the lowering of the metal Fermi level by an amount $|q|V_G$ relative to the equilibrium position. As a result, the oxide conduction band is tilted in the opposite direction. The positive voltage on the metal requires a positive charge on the metal and a corresponding negative charge at the surface of the semiconductor. Such a negative charge in the p-type material arises from the depletion of holes from the region near the surface, and hence uncovering enough negative ions. Band bending takes place in the semiconductor such that E_V moves away from E_{F_s}, or E_{F_i} bends toward E_{F_s} (making $E_{F_i} - E_{F_s}$ smaller). This means less p at the surface than inside the bulk p material (Fig. 3.5b). If we continue to increase the positive voltage, the bands in the semiconductor bend more strongly (Fig. 3.5c). At a sufficiently large voltage, E_{F_i} is much closer to E_c than E_V at the surface. This means the material at the surface becomes more n-type than p-type. At the crossover when $E_{F_i} = E_{F_s}$ the material is intrinsic. The electron concentration at the surface n_s is given by

$$n_s = n_i e^{\left(E_{F_s} - E_{F_{is}}\right)/kT} \tag{3-23}$$

where $E_{F_{is}}$ is the intrinsic Fermi level at the surface. In fact, the region from the crossover point all the way to the surface is called the inversion layer, which is an n-type region formed due to the strong applied positive gate voltage. In fact, it comes about due to the need for gathering more negative charges at the semiconductor surface. Since, negative ions uncovered by the depletion of holes are not enough to build up enough negative charges, the rest comes about from the enhancement of electrons at the surface of the semiconductor, hence called enhancement mode, and eventually forming an inversion layer (also called conduction channel, in this case n-channel).

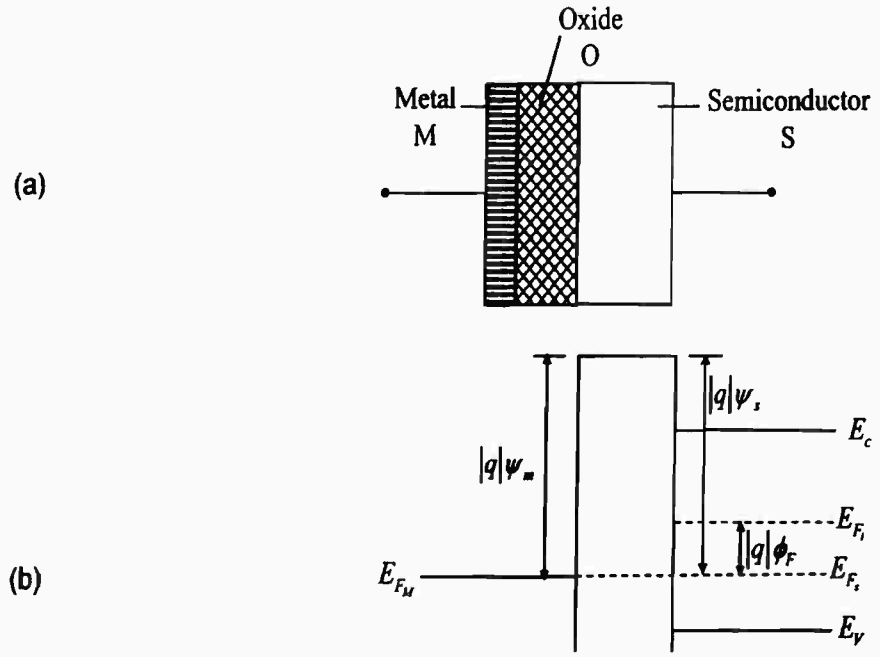

Fig. (3.4) MOS capacitor (p- type semiconductor) at zero voltage
a) MOS structure b) band diagram with $V_G = 0$, $\psi_m = \psi_s$

3.9 Strong Inversion

We shall take a closer look at the inversion layer. In Fig. (3.6) we have a case of strong inversion. Let us define potential ϕ at any point x measured from the bulk outwardly toward the surface relative to the equilibrium position of E_{F_i} which is E_{F_a} (inside the bulk of the semiconductor). The energy $|q|\phi$ gives the extent of the band bending at any x, and $|q|\phi_s$ represents the band bending at the semiconductor surface, while $|q|\phi_F$ measures the difference between E_{F_a} (E_{F_i} in the bulk) and E_{F_s}. Thus $|q|\phi_F = E_{F_a} - E_{F_s}$.

We call the case when $\phi_s = 0$ (Fig. 3.4) flat band condition. When $\phi_s < 0$ the bands bend up at the surface and we have hole accumulation (Fig. 3.5a). When $\phi_s > 0$ we have hole depletion (Fig. 3.5b). When ϕ_s is positive and $\phi_s = \phi_F$ we have crossover or start of inversion. When ϕ_s is positive and $\phi_s > \phi_F$, E_{F_i} lies below E_{F_s} and inversion is obtained. A good criterion for strong inversion is $\phi_s = 2\phi_F$ i.e., E_{F_i} lies sufficiently below E_{F_s} to ensure strong inversion. From eqn. (3-22), the condition of strong inversion ϕ_{sinv} is given using $p_0 = N_A$ in the bulk by

$$\phi_{sinv} = 2\phi_F = 2\frac{kT}{|q|} ln \frac{N_A}{n_i} \qquad (3\text{-}24)$$

For equilibrium concentration with E_{F_a} is intrinsic Fermi level in the bulk

$$n_0 = n_i e^{(E_{F_i} - E_{F_a})/kT} = n_i e^{-q\psi_F/kT} \qquad (3\text{-}25)$$

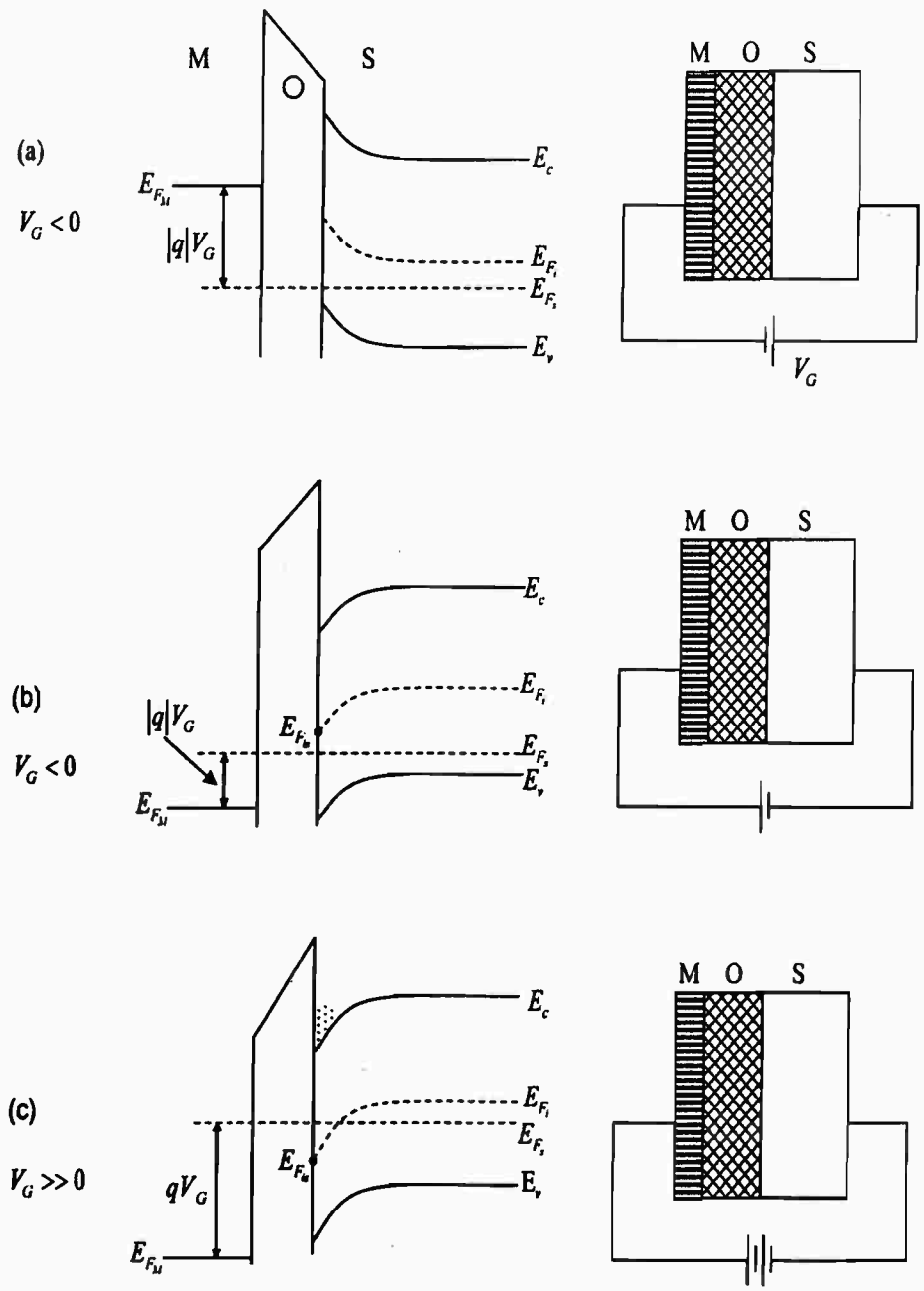

Fig. (3.5) MOS with external voltage

a) $V_G < 0$ *(accumlation)* **b)** $V_G > 0$ *(depletion)* **c)** $V_G >> 0$ *(inversion)*

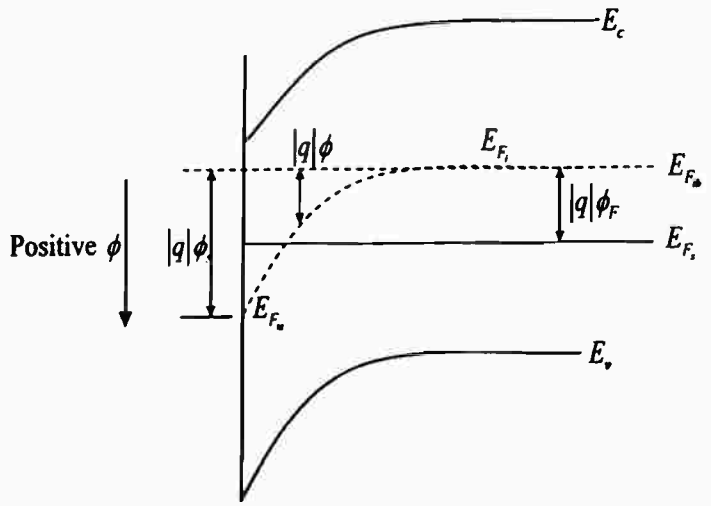

Fig. (3.6) Strong inversion

Whereas for every x with

$$E_{F_i}(x) = E_{F_n} - q\phi(x) \tag{3-26}$$

$$n(x) = n_i e^{(E_{F_n} - E_{F_i}(x))/kT}$$

$$= n_i e^{(E_{F_n} - E_{F_n})/kT} e^{q\phi(x)/kT}$$

$$n(x) = n_0 e^{q\phi(x)/kT} \tag{3-27}$$

Similarly for holes

$$p(x) = p_0 e^{-q\phi(x)/kT} \tag{3-28}$$

3.10 Threshold Voltage

From basic physics space charge is governed by Poisson's equation

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\varsigma(x)}{\epsilon_s} = -\frac{d\varepsilon(x)}{dx} \tag{3-29}$$

Where $\varepsilon(x)$ is the electric field, $\varsigma(x)$ is the charge density and ϵ_s is the dielectric constant of the semiconductor and $\varsigma(x)$ is given by

$$\varsigma(x) = |q|\left(N_D^+ - N_A^- + p - n\right) \tag{3-30}$$

The charge distribution, electric field and electrostatic potential for the inverted surface are sketched in Fig. (3.7). We assume complete depletion for $0 < x < W$ and neutral material for $x > W$ (in the bulk), x here being measured from the surface toward the bulk. This equation helps us calculate the electric field and the electrostatic potential profiles. This is usually done by calculating $\frac{d\varepsilon(x)}{dx}$ from the knowledge of $\varsigma(x)$ taking the dominant component (usually ion concentration N_D^+ or N_D^-). $\phi(x)$ is the integral (area) under $\varepsilon(x)$. So we may calculate $\Delta\phi$ as the total area under $\varepsilon(x)$ curve. In this case the charge due to uncompensated acceptors in the depletion region is $-|q|N_A WA$ where A is the cross sectional area. The

positive charge Q_m on the metal is balanced by the negative charge Q_s in the semiconductor, which is the depletion layer charge Q_d plus the charge in the inversion region Q_n.

$$Q_m = -Q_s = -(Q_d + Q_n) \tag{3-31}$$

$$|Q_s| = (|q|N_A WA + Q_n) \tag{3-32}$$

The inversion layer is generally less than 100Angstron (A). In Fig. (3.7c,d) we neglect the presence of this layer at the start of inversion. We note that the supplied voltage V_G appears potentially across the insulator (V_{ox}) and partially across the depletion layer (ϕ_s), i.e.,

$$V_G = V_{ox} + \phi_s \tag{3-33}$$

The voltage across the insulator is related to the charge on either side divided by the capacitance

$$V_{ox} = \frac{Q_m}{C_{ox}} = -\frac{Q_s}{C_{ox}} = -\frac{Q_s}{\epsilon_{ox} A} d_{ox} \tag{3-34}$$

where ϵ_{ox} is the permittivity of the insulator, d_{ox} is the oxide thickness and C_{ox} is the insulator capacitance. If we consider the width of the inversion layer to be small enough to neglect Q_n with respect to Q_d in eqn. (3-31) (called the depletion approximation) it can be shown (Prob. 3.2) that $\phi_s = \frac{1}{2}\varepsilon_{sm} W_m$ (Fig. 3.7d). Noting $N_A > N_D$, p, n in eqn. (3-30) then

$$W = \left(\frac{2\epsilon_s \phi_s}{|q| N_A} \right)^{1/2} \tag{3-35}$$

This depletion region grows with increased voltage V_G and hence ϕ_s. The maximum value for ϕ_s according to the depletion approximation - and hence the maximum value of depletion width W - may then be expressed using (eqn. 3-24) as

$$W_m = \left(\frac{2\epsilon_s \phi_{sinv}}{|q| N_A} \right)^{1/2} \tag{3-36}$$

$$= 2\left(\frac{\epsilon_s kT \ell n(N_A/n_i)}{|q^2| N_A} \right)^{1/2} \tag{3-37}$$

The charge in the depletion region Q_d at strong inversion is given by

$$Q_d = -|q| N_A W_m A = -2(\epsilon_s |q| N_A \phi_F)^{1/2} A \tag{3-38}$$

The applied voltage must be large enough to create this depletion charge plus the surface potential ϕ_{sinv}. The threshold voltage V_G required for strong inversion V_T using eqns. (3-24), (3-33) and (3-34) is given by

$$V_T = -\frac{Q_d}{C_{ox}} + 2\phi_F \tag{3-39}$$

In this analysis we have assumed that the negative charge at the semiconductor surface at inversion is mostly due to the depletion charge Q_d even at the condition called strong inversion ($\phi_{s_{inv}} = 2\phi_F$). The threshold voltage represents the minimum voltage required to achieve strong inversion or establishing a channel (strong inversion). It is an extremely important quantity for MOS transistors (Chapter 7).

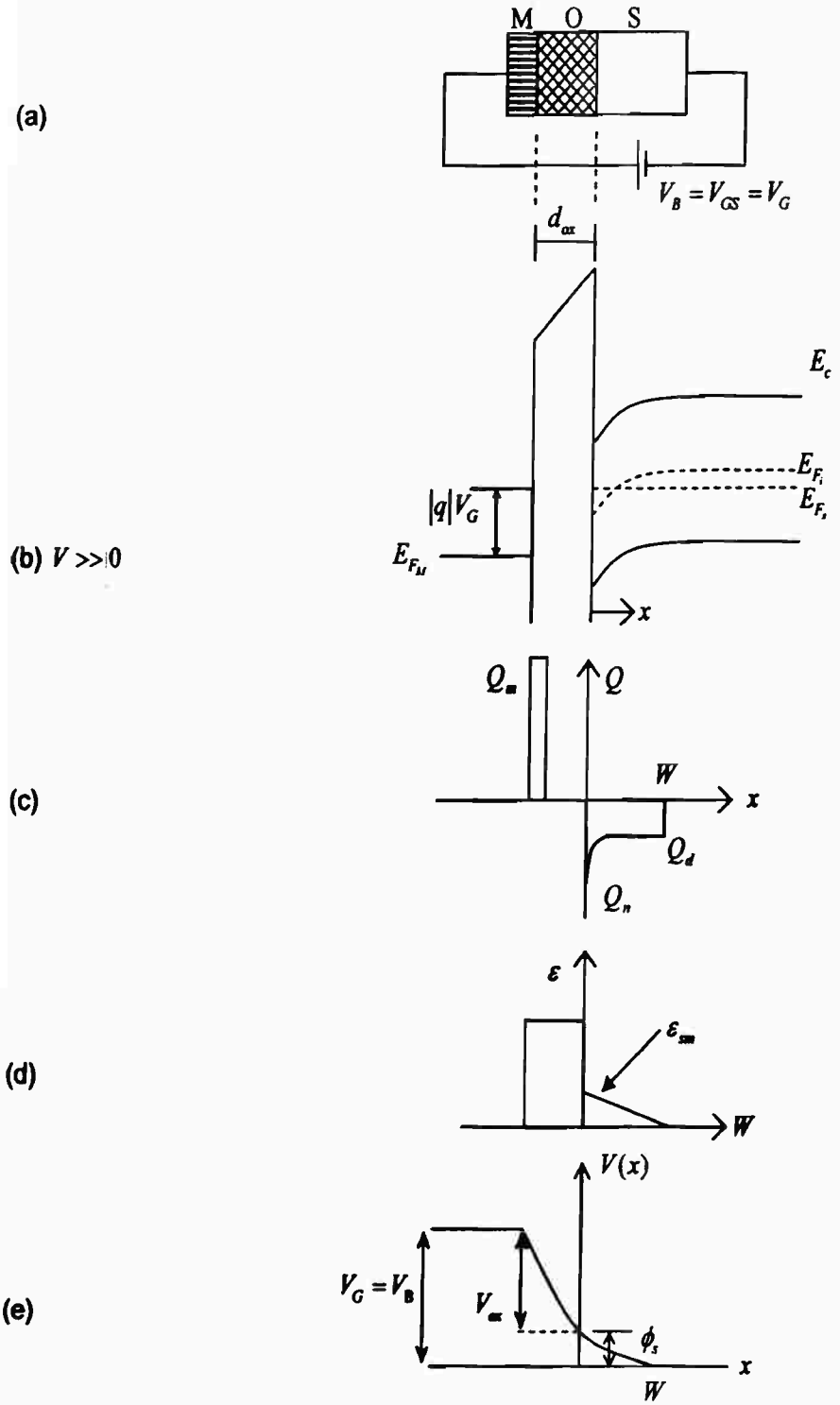

Fig. (3.7) Distribution of charge, electric field and electrostatic potential in an ideal MOS capacitor in inversion

a) circuit b) band diagram c) charge distribution
d) electric field e) electrostatic potential

3.11 Capacitance Voltage Characteristics

We may now investigate the variation of capacitance with V_G, called capacitance voltage characteristics (Fig. 3.8). The C-V characteristics vary depending on the semiconductor being in accumulation, deleption or inversion. For negative voltages, holes are accumulated at the surface of the semiconductor and MOS structure appears almost like a parallel plate capacitor dominated by the insulator capacitance

$$C_{ox} = \frac{\epsilon_{ox} A}{d_{ox}} \tag{3-40}$$

As V_G becomes positive the semiconductor is depleted, a depletion layer capacitance C_d is added in series with C_{ox}, where

$$C_d = \frac{\epsilon_s A}{W} \tag{3-41}$$

Where ϵ_s is the semiconductor permittivity and W is the width of the depletion layer (eqn. 3-35). Thus the total (series) capacitance is

$$C = \frac{C_{ox} C_d}{C_{ox} + C_d} \tag{3-42}$$

This capacitance decreases with positive V_G as W grows until finally inversion is reached at V_T. With inversion there is no further charge in C_d since the depletion width has reached its maximum W_m (eqn. 3-36). If instead of using dc voltages, very low frequency (10Hz) voltages are used, electrons in the n channel rather than fixed ions in the depletion region respond to the varying ac voltage and the structure behaves again as a parallel plate capacitor. Because of this effect during measurement at very low frequency, a MOS capacitor in inversion resembles a parallel plate capacitor C_{ox} (dashed line in Fig. 3.8).

Ex. 3.1

An ideal MOS capacitor has $N_A = 10^{16} cm^{-3}$ and $100A^{\circ}$ thick S_iO_2. Calculate the major points on the C-V curve (Fig. 3-8). The relative dielectric constant for S_i is 11.8, and of S_iO_2 is 3.9 and the permittivity of air is $8.85 \times 10^{-14} F/cm^2$. Take the area to be $1cm^2$.

Solution

$$C_{ox} = \frac{\epsilon_{ox}}{d_{ox}} = \frac{(3.9)(8.85 \times 10^{-14})}{10^{-6}} = 3.45 \times 10^{-7} F/cm^2$$

$$\phi_F = \frac{kT}{|q|} \ell n \frac{N_A}{n_i} = 0.0259 \ell n \left[\frac{10^{16}}{4.5 \times 10^{10}} \right] = 0.347V$$

Using eqn. (3-37), noting $\phi_{s_{inv}} = 2\phi_F$

$$W_m = 2\sqrt{\frac{\epsilon_s \phi_F}{|q| N_A}} = 2\left[\frac{(11.8)(8.85 \times 10^{-14}) \times (0.347)}{(1.6 \times 10^{-19})(10^{16})} \right]^{1/2}$$

$$= 3.01 \times 10^{-5} cm = 0.301 \mu m$$

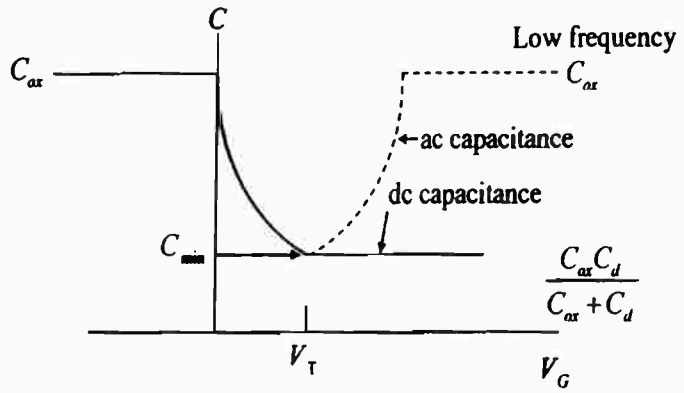

Fig. (3.8) Capacitance voltage characteristic for an ideal n channel (p substrate) MOS capacitor. The dashed curve for $V_G > V_T$ is observed only at very low measurement frequencies

$$Q_d \text{ per unit area} = -|q| N_A W_m = -\left(1.6\times10^{-19}\right)\left(10^{16}\right)\times\left(0.301\times10^{-4}\right)$$
$$= -4.82\times10^{-8}\, C/cm^2$$

Using eqn. (3-39)

$$V_T = -\frac{Q_d}{C_{ox}} + 2\phi_F = \frac{4.82\times10^{-8}}{34.5\times10^{-9}} + 2(0.347) = 0.834\text{V}$$

At V_T applied

$$C_d \text{ per unit area} = \frac{\epsilon_s}{W_m} = \frac{(11.8)\left(8.85\times10^{-14}\right)}{0.301\times10^{-4}} = 3.47\times10^{-8}\, F/cm^2$$

Using eqn. (3-42)

$$C_{min} = \frac{C_{ox}C_d}{C_{ox}+C_d} = \frac{34.5\times3.47\times10^{-9}}{34.5+3.47} = 3.15\times10^{-8}\, F/cm^2$$

This is a good way to determine V_T experimentally by locating the minimum of the C-V curve.

Problems

1- Verify eqns. (3-20) and (3-35).

2- Find the maximum width of the depletion region (just before inversion starts) for an ideal MOS capacitor on p-type S_i with $N_A = 10^{16} cm^{-3}$. Take the relative constant of S_i as 11.8 and the dielectric constant of air $8.85 \times 10^{-4} F/cm$.

3- Referring to Fig. (3.8) what happens when the voltage is ac at high frequency and why.

4- Calculate V_T for the MOS structure in Ex. 3.1.

5- Demonstrate the effect of varying N_A on V_T.

6- Obtain and sketch the distributions of charge, electric field and electrostatic potential in an ideal MOS capacitor in inversion.

7- Derive expressions for band bending, space charge, inversion layer charge, and inversion layer width for $V_G > V_T$.

8- Find the threshold voltage for S_i n channel MOS capacitor for $N_A = 10^{17} cm^{-3}$ and oxide thickness $200 A^o$.

9- Redo the above problem for p channel device.

10-Can we use C-V measurement to determine the position of Fermi level in a semiconductor experimentally?

References

1- "Semiconductor Devices", S. M. Sze, 3rd edition, Wiley, N. Y., 2006.

2- "Solid State Electronic Devices", B. G. Streetman and S. K. Banerjee, 6th edition, Pearson, Prentice Hall, Upper Saddle River, N. J., 2006.

3- "Principles of Electronic Materials and Devices", S. O. Kasap, 2nd edition, McGraw Hill, N. Y., 2002.

4- "Electronic Devices and Circuit Theory", R. Boylestad, L. Nashelsky, 8th edition, Prentice-Hall, Upper Saddle River, N. J., 2002.

5- "Physical Foundations of Solid State and Electronic Devices", A Ferendeci, McGraw Hill, N. Y., 1991.

6- Electronic Devices and Circuits", T. Bogart, 2nd edition, Maxwell Macmillan, N. Y., 1991.

7- Electronic Devices", S. R. Fleeman, Prentice Hall, Upper Saddle River, N. J., 1990.

8- "Semiconductor Devices", M. Zambuto, McGraw Hill, N. Y., 1989.

9- "Integrated Circuits: Materials, Devices and Fabrication", W. C. Till and J. T. Luxon, Pentice Hall, Englewood Cliffs, N. J. 1982.

10-"Solid State Physical Electronics", A. van der Ziel, 3rd edition, Prentice-Hall, Englewood Cliffs, N. J., 1976.